CLAIMS

1. (Currently Amended) A phase synchronizer comprising:

an input shift register for receiving a sequence of bits ~~containing~~ comprising a codeword;

a first syndrome computing module, operatively coupled to said input shift register, for computing first syndromes relating to a first potential phase of said codeword;

a first error detection module for determining, based upon said first syndromes, a first number of errors associated with said first potential phase of said codeword;

a second syndrome computing module, operatively coupled to said input shift register, for computing second syndromes relating to a second potential phase of said codeword;

a second error detection module for determining, based upon said second syndromes, a second number of errors associated with said second potential phase of said codeword; and

a comparator arrangement for comparing said first number of errors and said second number of errors to a threshold value, said first potential phase corresponding to a valid codeword phase when said first number of errors is less than said threshold value and said second potential phase corresponding to a valid codeword phase when said second number of errors is less than said threshold value.

2. (Original) The phase synchronizer of claim 1 wherein said first error detection module generates an error location polynomial using said first syndromes, said error location polynomial being of an order corresponding to said first number of errors.

3. (Currently Amended) A codeword synchronization module comprising:

an input shift register for receiving a sequence of bits ~~containing~~ comprising a codeword;

a plurality of phase synchronizers associated with a corresponding plurality of potential phases of said codeword, each of said phase synchronizers producing a codeword valid signal upon determining that said input shift register includes a set of said bits corresponding to said codeword; and

a comparator coupled to said plurality of phase synchronizers to determine whether any of said phase synchronizers produce a codeword valid signal.

4. (Currently Amended) The codeword synchronization module of claim [4] 3 wherein a first of said phase synchronizers produces a codeword valid signal upon determining that a number of errors within an associated one of said potential phases of said codeword is less than a predefined threshold, said first of said phase synchronizers including:

a syndrome computing module; and

an error detection module, said error detection module determining a first number of errors associated with a first of said plurality of potential phases of said codeword using syndromes produced by said syndrome computing module.

5. (Original) The codeword synchronization module of claim 4 wherein said syndrome computing module is reset in accordance with said first of said plurality of potential phases.

6. (Original) The codeword synchronization module of claim 5 wherein said error detection module is actuated prior to resetting of said syndrome computing module.

7. (Currently Amended) The codeword synchronization module of claim 4 wherein said first of said phase ~~synchronizer~~ synchronizers includes a comparator coupled to said error detection module, said comparator producing one of said codeword valid signals when said first number of errors is less than said ~~predetermined~~ predefined threshold.

8. (Original) The codeword synchronization module of claim 4 wherein said error detection module generates an error location polynomial using syndromes produced by said syndrome computing module and wherein an order of said error location polynomial corresponds to said first number of errors.

9. (Original) A method of codeword synchronization comprising:

computing first syndromes relating to a first potential phase of a received codeword;

determining, based upon said first syndromes, a first number of errors associated with said first potential phase of said codeword;

computing second syndromes relating to a second potential phase of said codeword;

determining, based upon said second syndromes, a second number of errors associated with said second potential phase of said codeword; and

comparing said first number of errors and said second number of errors to a threshold value, said first potential phase corresponding to a valid codeword phase when said first number of errors is less than said threshold value and said second potential phase corresponding to a valid codeword phase when said second number of errors is less than said threshold value.

10. (Original) The method of codeword synchronization of claim 9 wherein said determining said first number of errors includes generating an error location polynomial using said first syndromes, said error location polynomial being of an order corresponding to said first number of errors.

11. (Currently Amended) A method of codeword synchronization comprising:

receiving a sequence of bits ~~containing~~ comprising a codeword;

computing a plurality of sets of syndromes, each set of syndromes being associated with a potential phase of said codeword;

identifying a number of errors associated with each said potential phase of said codeword using the one of said sets of syndromes associated with each said potential phase; and

determining whether a number of errors associated with any of said potential phases is less than a predetermined threshold.

12. (Original) The method of codeword synchronization system of claim 11 wherein said identifying includes generating an error location polynomial corresponding to a first of said potential phases using a first of said sets of syndromes wherein an order of said first error location polynomial corresponds to a first number of errors associated with said first of said potential phases.

13. (Currently Amended) A data receiving apparatus for receiving data packets, each of said data packets being identified by an access code, said apparatus comprising:

an input shift register for receiving a sequence of bits ~~containing~~ comprising a codeword, said codeword corresponding to one of said access codes; and[,]

a plurality of codeword detection modules associated with a corresponding plurality of potential phases of said codeword, each of said codeword detection modules generating a codeword valid signal when a number of errors associated with an associated one of said potential phases is less than a predetermined threshold.

14. (Original) The data receiving apparatus of claim 13 further including an error correction circuit for carrying out an error correction operation on said codeword using error correction information provided by ones of said codeword detection modules generating codeword valid signals.

15. (Original) The data receiving apparatus of claim 14 wherein each of said codeword detection modules is operative to compute a predefined number of syndromes of a different one of said plurality of potential phases of said codeword.

16. (Original) The data receiving apparatus of claim 15 wherein said error correction uses said predefined number of syndromes from a first of said codeword detection modules to determine one or more bit positions of erroneous bits within said sequence of bits and to correct said erroneous bits.

17. (Currently Amended) The data receiving apparatus of claim 15 ~~where~~ wherein each of said codeword detection modules includes:

a syndrome computing module for computing syndromes of said codeword;

an error detection module for determining, based upon said syndromes, a number of errors within said codeword; and

a comparator for comparing said number of errors to a threshold value, said codeword corresponding to a valid codeword when said number of errors is less than said threshold value.

18. (Currently Amended) The codeword synchronization ~~system~~ module of claim 3 further including an error correction circuit for carrying out an error correction operation on said codeword using error correction information provided by said plurality of phase synchronizers.

19. (Original) The method of codeword synchronization of claim 9 further including carrying out an error correction operation on said codeword on the basis of an error location polynomial derived from said first syndromes.

20. (Currently Amended) A codeword synchronization system comprising:

a sampling arrangement for generating N bitstreams in response to a received data stream, where N is an integer;

a set of N codeword synchronization modules, each of said N codeword synchronization modules providing a plurality of codeword error signals indicative of a number of errors associated with a corresponding plurality of potential phases of one of said N bitstreams; and

a phase selection module for identifying one of said codeword error signals as being indicative of a lowest number of errors.

21. (Original) The codeword synchronization system of claim 20 wherein a first of said set of N codeword synchronization modules includes:

an input shift register for receiving a first of said N bitstreams, said first of said N bitstreams containing a codeword, and

a plurality of syndrome computing modules, each of said syndrome computing modules computing syndromes being associated with a different one of said plurality of potential phases of said codeword.

22. (Currently Amended) The codeword synchronization system of claim 21 wherein said first of said set of N codeword synchronization modules further includes a plurality of error detection modules, each of said error detection modules determining a number of errors associated with a corresponding one said plurality of potential phases of said codeword using the syndromes produced by an associated one of said plurality of syndrome computing modules.

23. (Original) The codeword synchronization system of claim 20 wherein said sampling arrangement includes:

a sampling circuit; and

a clock coupled to said sampling circuit, said clock being operative at N times a data rate of said received data stream.

24. (Currently Amended) The codeword synchronization system of claim 23 wherein said sampling arrangement further includes a demultiplexer having an input port connected to said sampling circuit and a set of N output ports connected to said set of N codeword synchronization modules.